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An Efficient and High Speed 10 Transistor Full Adders with Lector Technique

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Abstract: *An Energy Efficient and high speed 10 Transistor with lector technique of full adder is proposed. The full adder consists of 10 transistors with only one type of logic style i.e., pass transistor logic style. The Low power and high speed full adder circuits are mostly used in portable applications. In comparing with the existing designs, the proposed design gives low power. The designs presented in this paper were simulated in CMOS 180nm and 45nm technology using Cadence tool, observed to have superior characteristics such as power consumption, power-delay-product(PDP) and layout area when compared to existing adders.*
Keywords: *Full adder, LECTOR technique, Pass Transistor logic*.

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I. Introduction

The researchers are developing the adder structure with different names such as full adder, Binary adder, carry look ahead adder etc. But developing of all these adders the basic structure of adder is full adder. The performance of all full adder [6] are same but the count of the transistor will be reduced or increased. The design style which are used in previous full adder are may be static design style or dynamic logic design style. When comparing with these two logic design styles the static design style is simple, easier. The logic design styles include its different parameters to discuss about the style. The standard Complementary Metal Oxide Semiconductor [2&3], Complementary Pass Transistor Logic [2&5], TFA [2&3], HPSC adder [1&9],24T Adder [6],4T XNOR [2], Parallel 4 FCA [8], SERF Adder [7].

This paper consists of five sections. Section I is introduction that presents the basic knowledge of adders. Section II presents the previously existing adders with their waveforms. Section III presents the latest work of 10 Transistor adder and comparison of existing Hybrid Full Adder with the proposed 10 Transistor Full Adder. Section IV concludes the paper.

II. Circuit Description

The Hybrid Full Adder is designed with 3 blocks which are named as modules in Figure. 1[4]. The Block 1and Block 2 both represents the XNOR. These two blocks are used to get the output signal1 and another block is used to get the output signal 2. In this Hybrid Full Adder every Block is used to get the accurate signals with respect to different parameters.

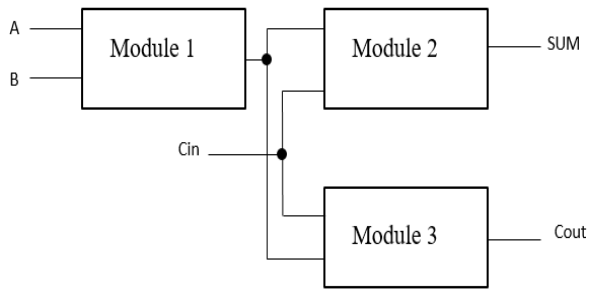

Figure 1: Structure of Adder with 3 Modules

i. Detailed Structure of Hybrid Full Adder

The detailed explanation of every block is discussed below in detail. The block 1 is the XNOR module which is shown in Figure. 2. The XNOR block modules are used to get the betterpower. At the stage of the output there is a Level Restoration Circuit. Because of the Level Restoration Circuit, the output signal can get the output with of full swings. And at the Input B there is a weak inverter, it is placed because of reducing of the width of transistor.

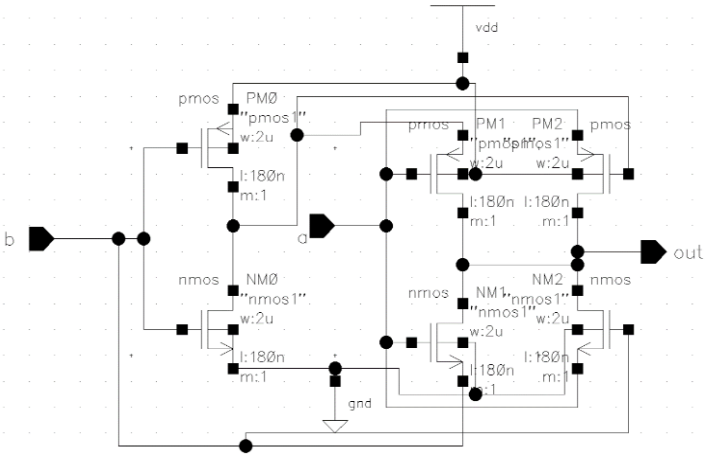

Figure 2: Schematic structure of XNOR Block

The Block 3 is the carry generation block which is shown in figure. 3. In this Transmission gate design style is presented due to of its advantage of reducing transistors and the delay can be reduced.

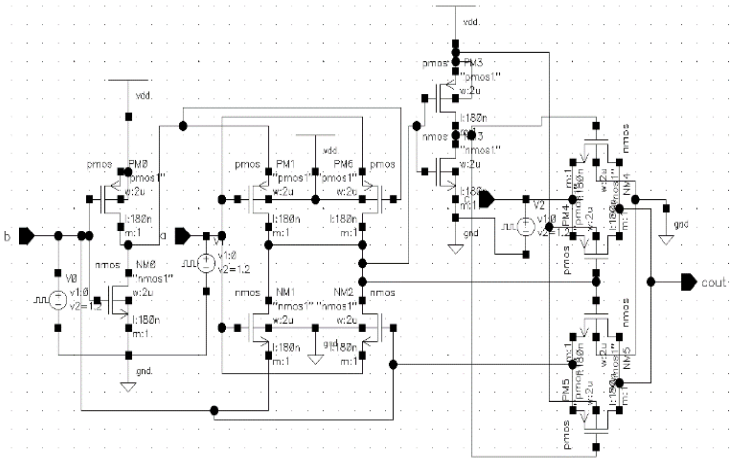

Figure 3: Schematic structure of Block 3

By Combining of all blocks the Hybrid Full Adder circuit which is represented in figure. 4. The Hybrid Full Adder Circuit uses two different logic styles which are used to get the accurate outputs with of good power consumption and delay.

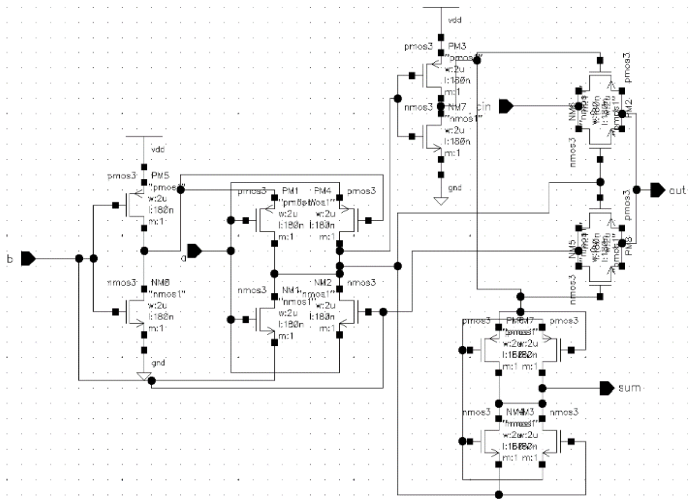

Figure 4: Schematic structure of Full Adder with two Logic Styles

The Output of the carry signal can also be represented as the signals input 1 and 2 are equal than the carry out signal will be same as that of the input 2 else it will be equal to the input 3. The detailed Explanation of Hybrid Full adder with respect to waveforms is represented in figure 5.
The Hybrid Circuit consists of 16 transistors with both the PMOS and NMOS. The layout of the Hybrid Full Adder circuit is represented in figure 6.

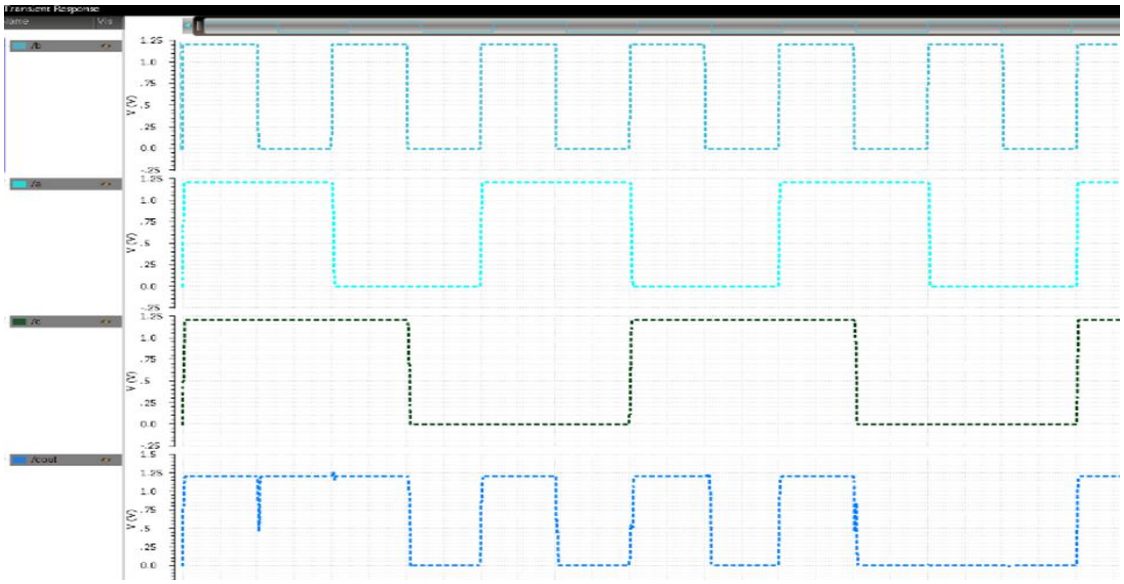

Figure 5: Waveforms of Hybrid Full Adder Circuit.

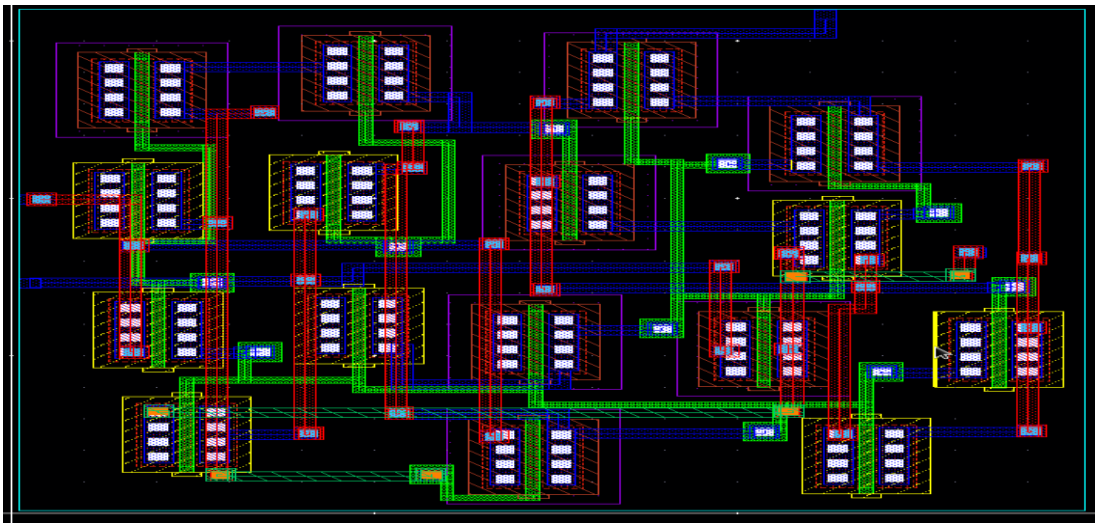

Figure 6: Layout of Hybrid Full Adder Circuit.

The Hybrid Full adder circuit can be taken as 1 Bit adder cell. The 1Bit adder cell is implemented to 32 bits. But these 32-bit adder cell is similar to that of Carry Ahead Structure. The 32 Bit Adder cell can be shown in figure 7.

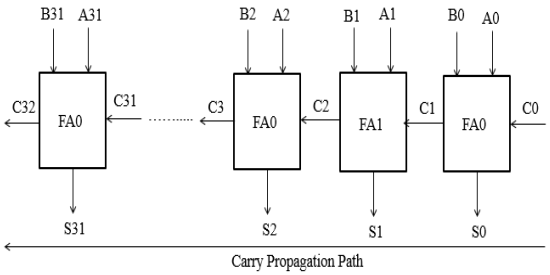

Figure 7:32 –Bit adder cell.

III. Full Adder Circuit With Of 10 Transistor

The16 transistor Hybrid full adder circuit [4] is modified to 10 Transistor which is shown in figure. 8. The 10 Transistor doesn't have any direct path to ground. Due to this advantage the power consumption can be reduced. In 10 Transistor circuit there are two XNOR circuits which are in cascaded form. In this circuit first sum signal is generated and then the carry out signal is generated through the transmission gate.

To get the better results of 10 Transistor an additional technique is added. The additional technique is LECTOR (Leakage Control Transistor) technique. In this technique there is two transistors additionally are kept to the circuit. The VDD supply and ground helps to get the power consumption as low.

The 10 Transistor with of LECTOR technique is shown in figure 9. The Transistor which are inserted in the circuit are controlled by the gate terminal of each transistor with their sources. Whenever the inputs A and B are given as high and low. The first two transistors will be off and second will be on in PMOS and NMOS, the XNOR module will can get the output of low.

The low output is given as the input to another cascaded XNOR module with additional input c. The input c is given as low, so the transistors PMOS are off and NMOS are on. The supply of VDD is directly goes to the sum signal. The input of c is low at the connection there is a signal of low input. So the carry signal will be of low carry out.

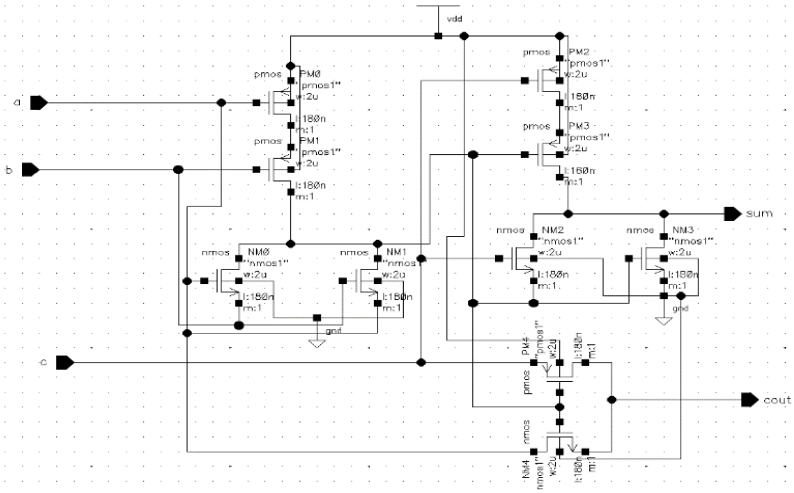

Figure 8: Schematic Structure of 10 Transistor

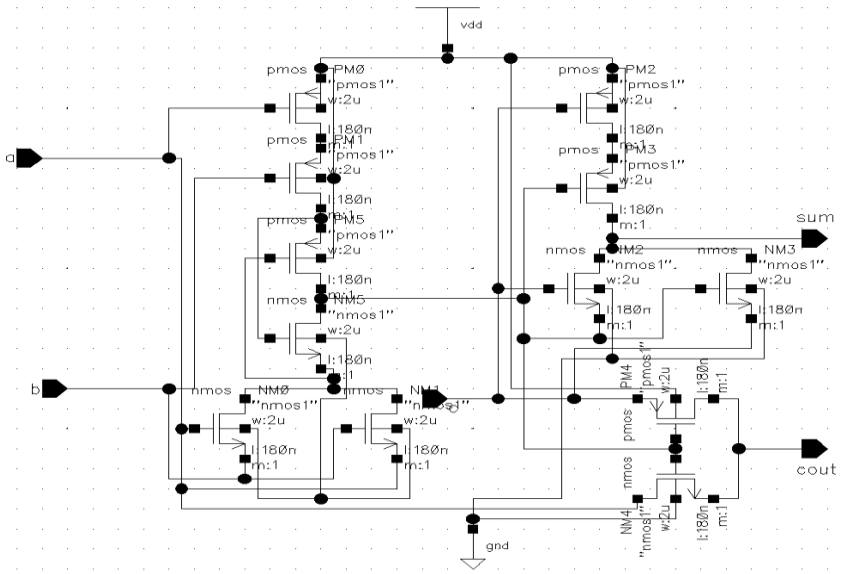

Figure 9: Schematic Structure of 10 Transistor with LECTOR technique

The simulation results of the 10 Transistor with LECTOR technique can be shown in figure 10 and layout is shown in the figure11. The simulation results show the proposed circuit can operate at higher speed with low power dissipation. From the comparison results the 10 Transistor full adder has efficient design which is shown in Table 1.

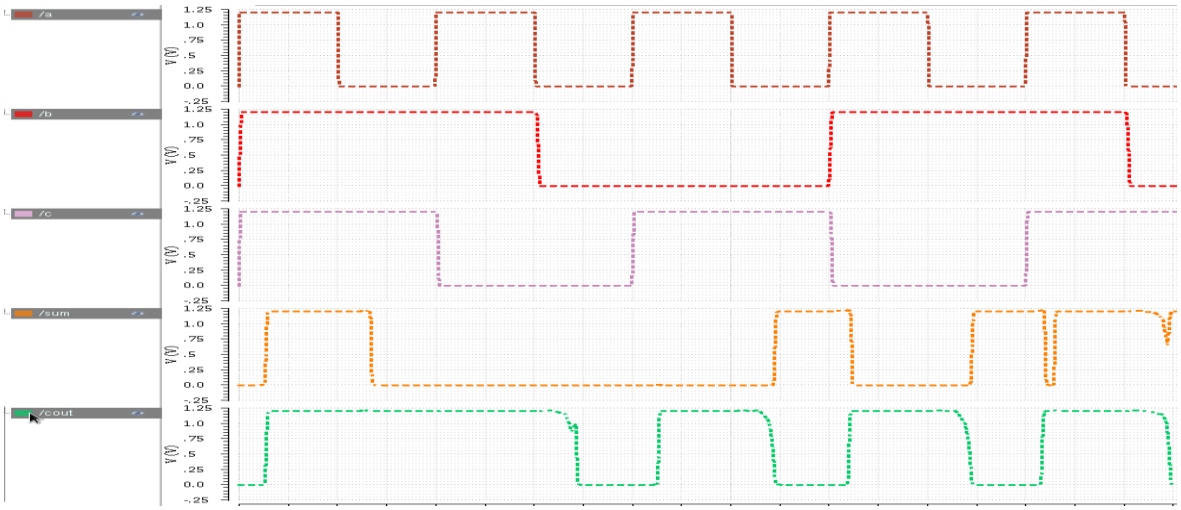

Figure 10: Waveforms of 10 Transistor with LECTOR technique.

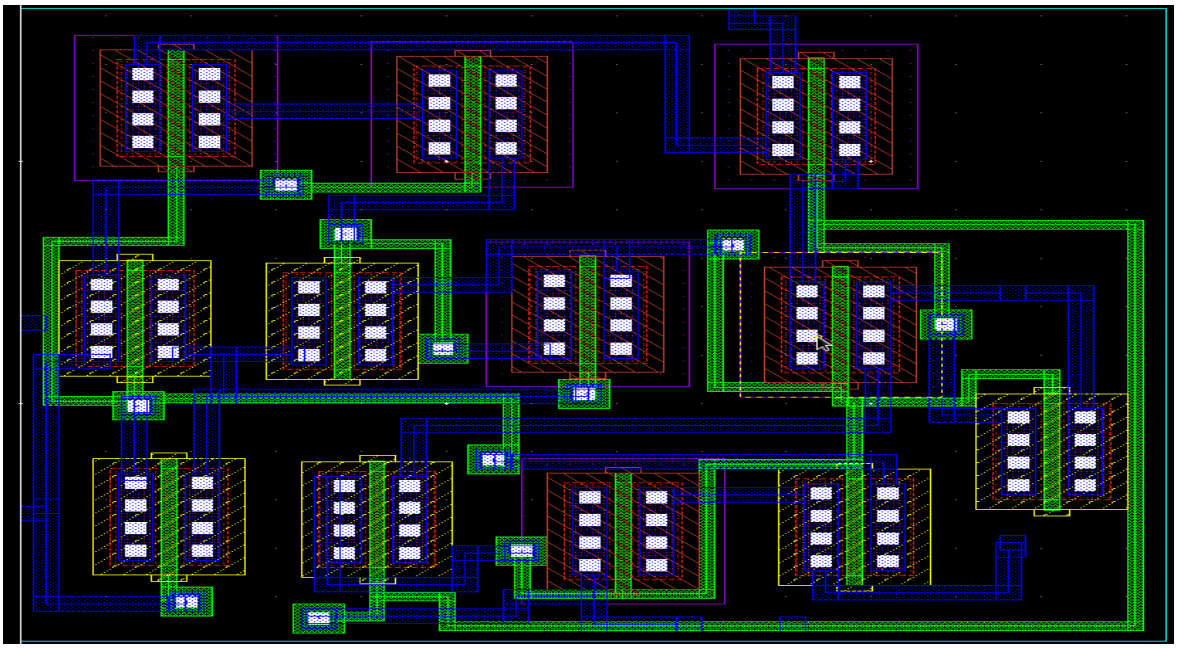

Figure 11: Layout of 10t Transistor with LECTOR technique.

Table1: Comparison of Layout Area

Circuit	Layout Area(um^2)	
	180nm	45nm
Hybrid 1 Bit Full Adder Circuit	236.9	3.92
10t Transistor with Lector technique	177.31	3.81

IV. Conclusion

The 10t transistor with LECTOR technique circuit has advantages of comparison with other circuits. The Area, Power and Delay is reduced with of the Hybrid Full Adder Circuit because of its circuit representation. Simulations results confirmed that the proposed circuit transistor count is reduced and power was reduced in comparison with existing designs. The circuits further can be designed and simulated using Advanced Cadence reduced technology which would be more advantageous.

References

[1] C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang: A low-power high-speed hybrid CMOS full adder for embedded system, in Proc.IEEE Conf.Design Diagnostics Electron. Circuits Syst., vol. 13, pp. 1–4, Apr. 2007.

[2] S. Wairya, G. Singh, R. K. Nagaria, and S. Tiwari: Design analysis of XOR (4T) based low voltage CMOS full adder circuit, in Proc. IEEENirma Univ. Int. Conf. Eng. pp. 1–7, Dec. 2011.

[3] R. Zimmermann and W. Fichtner: Low-power logic styles: CMOS versus pass-transistor logic, IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.
[4] P. Prashanth and P. Swamy: Architecture of adders based on speed, area and power dissipation, in Proc. World Conf. Inf. Commun.Technol. (WICT), pp. 240–244, Dec. 2011.
[5] M. J. Zavarei, M. R. Baghbanmanesh, E. Kargaran, H. Nabovati, and A. Golmakani: Design of new full adder cell using hybrid-CMOS logic style, in Proc. 18th IEEE Int. Conf. Electron., Circuits Syst. (ICECS), pp. 451–454,Dec. 2011.
[6] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei: A novel low-power full-adder cell for low voltage,VLSI J. Integr., vol. 42, no. 4, pp. 457–467, Sep. 2009.
[7] K. Navi et al., "A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter," Microelectron. J., vol. 40, no. 10, pp. 1441–1448, Oct. 2009.
[8] C. H. Chang, J. M. Gu, and M. Zhang: A review of 0.18-μm full adder performances for tree structured arithmetic circuits, IEEE Trans. VeryLarge Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 686–695, Jun. 2005.

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